High Performance Decimation Filter Design for Oversampling Delta-Sigma A/D Converters

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ABSTRACT

In this paper system design approach for high performance decimation filters is discussed. As a case study, we compared two algorithms for realization of decimation comb filters in respects of power consumption, speed and silicon area. Compared with the recursive algorithm, the significant advantage of non-recursive algorithm is its low power consumption and high speed in case of higher decimation filter orders and decimation ratios. Based on the non-recursive algorithm, a decimator with programmable orders (3rd, 4th and 5th), decimation factors (8, 16, 32 and 64) and input bits (1 and 2 bits) has been implemented in a 0.6 mm 3.3 V CMOS process.

INTRODUCTION

Oversampling delta-sigma analog-to-digital (A/D) converters have become very popular because with the aid of large digital decimation filters they avoid many difficulties encountered with conventional A/D converters [1][2]. For wide-band applications oversampling frequency increases from a few tens of MHz to GHz due to the high resolution requirement and wide bandwidth of analog input signals [7]. High speed decimation filters are needed. Meanwhile power consumption of the decimation filters will be very large at high oversampling frequency. Low power consumption will be a key problem [2][8][9][10]. Considering the integration with analog modulator, decimation filters with low digital noise are very important for the whole A/D converters. In-system programmability of decimation filter is also concerned to reduce power consumption due to the fact that different performance of decimation filters are required at different time in the communication systems. System design approach for high performance decimation filters which take into account above issues should be developed for future applications.

SYSTEM DESIGN APPROACH

Decimation filters can be designed with various structures (transfer functions), algorithms and technologies. System design approach is needed for selecting the structures, algorithms and technologies in the early design stage for low cost and short design cycle. Our main approach is try to analyse and compare different structures, algorithms and technologies at system level and get performance functions (in various formats, such as formula, curve, table, etc.) for them. For example, if the design target is low power consumption, we should get power consumption functions for different structures, algorithms and technologies. Based on the performance functions, we can quickly determine which structure, algorithm and technology should be employed for different system requirements.

CASE STUDY

We take recursive and non-recursive algorithms for decimation comb filters as a case study to demonstrate our design approach. First we compared these two algorithms at algorithm level and logic level in respects of power consumption, speed and silicon area. Then by using non-recursive algorithm, a low power programmable decimation comb filter was implemented in a 0.6 μm 3.3 V COMS process.

For VLSI implementations of multistage decimators [8][9][10][11], a computationally efficient first stage is provided by a comb filter [3][5] with following transfer function:

$$H(z) = \left(\sum_{i=0}^{N-1} z^{-i}\right)^k = \left(\frac{1-z^{-N}}{1-z^{-1}}\right)^k \qquad (1)$$

where N is the decimation ratio and k indicates the order of comb filter. One well-known algorithm for implementing comb filters is the recursive algorithm [1][4][6]. Another algorithm is the non-recursive algorithm [1].

With the commutative rule [1][6] the recursive algorithm with an IIR filter followed by a FIR filter is shown in Figure 2 [3][4][5]. The non-recursive algorithm utilized the commutative rule as well. Usually, the decimation ratio is chosen to be M-th power of 2. Then refer to equation (1), the non-recursive algorithm is shown in Figure 3.

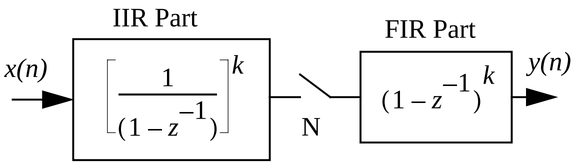


Figure 2: The recursive algorithm for comb filters

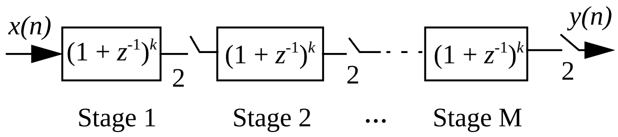
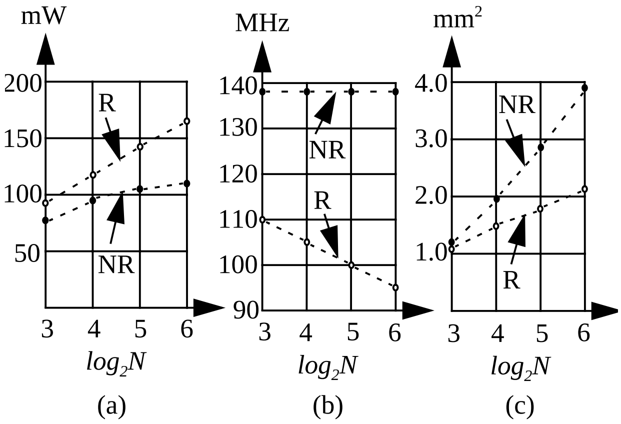


Figure 3: The non-recursive algorithm for comb filters



(a) Power consumption vs. decimation factor (70 MHz)
(b) Highest working frequency vs. decimation factor
(c) Size vs. decimation factor

Figure 4: Comparisons of the recursive (R) and non-recursive (NR) algorithms (When m = 1 and k = 5)

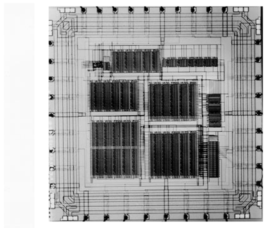


Figure 5: Die photo of the programmable decimation filter

To compare these two algorithms, we have finished some designs of comb filters (assuming $k = 5$, $N = 8, 16, 32$ and 64, and single-bit input) using both of recursive and non-recursive algorithms with a 0.6 μm 3.3 V CMOS process. We show the comparisons in Figure 4. It's clearly shown that the non-recursive algorithm is suitable for the low power and high speed comb decimator designs, and the recursive algorithm can be utilized for a compact design with modest performance, especially when decimation factor is large.

Based on above comparison, a low power comb decimator with programmable orders (3rd, 4th and 5th), decimation factors (8, 16, 32 and 64) and input bits (1 and 2 bits) by using non-recursive algorithm has been implemented in a 0.6 μm 3.3 V CMOS process. Figure 5 shows the die photo of the comb decimator. Its measured core power consumption is 44 mW at 25 MHz input data rate, and the highest input data rate is larger than 110 MHz.

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